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1. Title of the Invention

Method of manufacturing a semiconductor device

2. Scope of the Claim for Patent

(1) A method of manufacturing a semiconductor device by forming a resistive element to a polycrystal silicon layer on a semiconductor substrate in which one or more of oxygen and nitrogen is ion-implanted to a resistor element region of the polycrystal silicon layer.

(2) A method of manufacturing a semiconductor device as defined in claim 1, comprising a step of coating a portion of a surface of a polycrystal silicon layer to which impurities showing electro- conductivity are previously added with a film serving as a mask upon ion implantation and a step of implanting ions into the polycrystal silicon layer of the device element region exposed not covered with the mask after said step.

(3) A method of manufacturing a semiconductor device as defined in claim 1, wherein one or more of phosphorous,

boron and arsenic is used as impurities showing the electroconductivity.

(4) A method of manufacturing a semiconductor device as defined in claim 1, wherein the method comprises a step of covering a portion of the surface of the polycrystal silicon with a film to which impurities showing electroconductivity are added, a step of implanting ions to a polycrystal silicon layer of a resistor element region exposed not covered with a mask after said step, and a step of thermally diffusing impurities from the impurity-added layer to the polycrystal silicon layer.

(5) A method of manufacturing a semiconductor device as defined in claim 1, wherein the resistor element region of the polycrystal silicon layer is formed by way of a silicon oxide film on a substrate.

(6) A method of manufacturing a semiconductor device as defined in claim 1, wherein the ion implantation is conducted at a dose rate of 10^{12} /cm^2 - 10^{18}/cm^2.

3. Detailed Description of the Invention

The present invention concerns a method of manufacturing a semiconductor device using polycrystal silicon to a resistive element.

A semiconductor device having a resistive element as outlined in Fig. 1 has been known so far. That is, a silicon oxide film 12 and a polycrystal silicon layer 13 to

which impurities such as phosphorous are added in a slight amount as a resistive element are deposited on a semiconductor substrate 11, and a resistive element portion of the polysilicon layer 13 is covered with a silicon oxide film 14. Then, impurities showing electroconductivity such as phosphorus are sufficiently thermally diffused to the polysilicon layer 13 on both ends of the resistive element portion using the oxide silicon film 14 as a diffusion mask to form electrodes 15, 15' in ohmic contact with both ends of the resistive element. However, if it is intended to form a resistive element of a predetermined length (l), since the diffusion coefficient of the impurities showing the conductivity in the polycrystal silicon is large and the impurities diffuse also laterally upon thermal diffusion for forming the electrodes 15, 15' as far as to the beneath of the mask 14. For example, they laterally diffuse by 2μm during thermal diffusion at 1000°C for 20 min. Accordingly, the mask 14 requires a size of L + 4μm considering the diffusion, so that more than 5μm of a mask pattern is required for the resistive element to hinder the microrefinement.

Further, it is difficult to obtain more than 1 MΩ of the resistance value for the resistive element. This is because the electroconductive mechanism of polysilicon changes depending on the properties of the grain boundary along

which crystal grains are in contact with each other and significantly undergoes the effect of glowing conditions of polysilicon and conditions for thermal treatment as is well-known. For example, during deposition of the polysilicon film in an impurity atmosphere, the conditions for the amount of impurities and growth of polysilicon act simultaneously making it impossible to control the resistance value at a good accuracy. Particularly, if the amount of the impurities added, is small (high resistivity), change of the resistance value is abrupt and the controllability is poor. The situation is the same also in a case of adding impurities after the deposition of polysilicon. Accordingly, the upper limit for the resistance value which can be put to practical use is 1 MΩ at the greatest.

The present invention has been accomplished in view of the foregoing situations and provides a method of manufacturing a semiconductor device by forming a resistive element to a polycrystal silicon layer on a semiconductor substrate, wherein one or more of oxygen and nitrogen is ion implanted to the resistor element region of the polycrystal silicon layer thereby capable of forming a high resistance element of a high integration degree at a high accuracy.

The present invention is suitable to formation of a high resistance element of 1kΩ to 10^5 MΩ.

The present invention will be explained more specifically by way of a preferred embodiment with reference to the drawings.

Fig. 2 C shows a resistive element formed by one embodiment according to the present invention, in which a polysilicon layer 23, for example, of 5000Å thickness is deposited by way of a silicon oxide film 22 of 1μm thickness on a semiconductor substrate, for example, a p-type silicon substrate 21. A portion of the polysilicon layer 23 is covered with a silicon oxide film 24 and polysilicon electrodes 25, 25' to which impurities, for example, phosphorus are added at a high concentration, for example, of $10^{21}cm^{-2}$ is formed below the film 24, while oxygen or nitrogen is ion implanted into the polysilicon layer 23 exposed between the electrodes 25, 25' to form a resistive element. In the ion implanted region, the resistivity is increased in accordance with the dosing amount.

The resistive element is manufactured by a method, for example, as shown below. That is, after forming the silicon oxide film 22 of 1 μm thickness on the p-type silicon substrate 21, a phosphorus-added polysilicon layer 23 is deposited, for example, in phosphorous atmosphere by the CVD process. Then, after patterning the phosphorus-added polysilicon layer 23 (Fig. 2a), both end electrode portions thereof are covered with a silicon oxide film 24 (Fig. 2b)

and then one or more of oxygen (O) or nitrogen (N) ions, for example, oxygen ions are implanted to the phosphorus-added polysilicon layer 23 using the silicon oxide film 24 as a mask (Fig. 2C). After ion implantation, heating may be applied entirely. In the ion implanted region, SiO_x ($x \leq 2$) or Si_3N_x ($x \leq 4$) or both of them are formed to increase the resistivity. The dose amount is preferably from 10^{12} to $10^{18}/cm^3$, for example, $5 \times 10^{16}/cm^3$.

The size of the resistive element is substantially identical with the mask size of the silicon oxide film 24. This is because the diffusion of additional phosphorus from the electrode portion is negligible in the region in which oxygen or nitrogen is ion implanted since the property is remarkably different from that of polysilicon before ion implantation, because ion implantation has a straight forward nature, because oxygen or nitrogen is less diffusible in the lateral direction during heat treatment since the diffusion coefficient of oxygen or nitrogen is less than 1/10 compared with impurities showing conductivity such as phosphorus or the like. As described above, the accuracy for the size of the resistive element is also high, that is, the accuracy of the resistive value is also high.

Further, the length for one side of the resistive element can be made to a minimum size for allowing the patterning of the silicon oxide film mask 24, for example,

less than 3μm according to the photoengraving method for instance.

This means that refinement indeed by about several times can be attained as compared with the conventional method requiring from 7 to 9 μm mask size in order to obtain a resistive element of 3μm size.

Further, ion implantation of nitrogen or oxygen which is a main factor for determining the resistance value of the resistor element can be controlled for the resistance value independent of the growing condition for polysilicon layer. That is, when high resistivity is obtained for the resistive element of the prior art. The controllability for the resistance of the polysilicon layer is poor due to the growing condition of the polysilicon layer and the introduction of a small amount of impurities. On the contrary, in this embodiment, a desired high resistance value can be attained with good accuracy, because impurities showing electroconductivity are added by a considerable amount to the polysilicon layer thereby once reducing the resistivity to such an extent that the resistor functions as the wiring and then oxygen or nitrogen is ion implanted by a considerable amount by gradually increasing the resistance by an ion injection method having good controllability for the dose amount.

A particularly high resistivity can be attained by

adopting the following means. That is, a high resistance element may also be obtained by depositing a no-impurity added polysilicon layer, coating both ends with an impurity-added film, for example, a PSG film, one or more of oxygen and nitrogen is ion implanted to the exposed polysilicon layer using the PSG film as a mask and heating is applied entirely. In this case, phosphorus is diffused from the PSG film to the polysilicon layer in adjacent with both ends of the resistive element to function as an electrode. Since the ion implanted polysilicon has the property changed remarkably and can suppress the diffusion, phosphorus diffusion from the electrode portion is negligible.

The polysilicon layer described above may contain boron or arsenic instead of phosphorus, or may contain two or more of them.

Fig. 3 and Fig. 4 show wiring examples of the resistive element described previously. That is, aperture may be formed to electrode portions 25, 25' of a resistive element covered additionally with a silicon oxide film 31 and AL wirings 32, 32' may be connected with the electrode 25, 25' (Fig. 3). On the other hand, the electrode 25 may be in contact with a region 41 of a conduction type opposite to that of the substrate formed on the surface of a semiconductor substrate 21 (Fig. 4).

Further, as shown in Fig. 5, an AL wiring 32' formed on

the electrode 25' may be extended on the ion implantation region, which is advantageous in view of increased integration degree and pattern accuracy.

This is because current flows from the AL wiring layer 32' always by way of the electrode 25'

shows an example of coupling the resistor element with a MOS type transistor which comprises a resistor element, an impurity-added polysilicon gate electrode 62 formed on a gate oxide film 61, a source 63 and a drain, that is, a region 41 having an electroconductivity opposite to that of a substrate connected with a resistor element illustrated in Fig. 4.

Fig. 7 shows a static operation type flip-memory cell having, as a constitutional unit, a device comprising the transistor and the resistor element shown in Fig. 6. That is, Tr1 through Tr4 are transistors in which Tr3 and Tr4 are switching transistors for establishing conduction between bit lines DL, DL and a memory cell in accordance with pulses from word line WL. The resistors R_1 and R_2 form load resistors for the transistors Tr1, Tr2 respectively and form current path successively from power source terminal V_{DD} to terminal V_{ss} to attain a bistable state. Since Tr1 and R1 or Tr2 and R3 are constituted as shown in Fig. 5, they can be integrated at an extremely high density. In addition, since high resistivity can be obtained for R1 and R2, low electric

power consumption can be attained.

For example, in the existent resistor element, since R_1 and R_2 are 1 MΩ at the greatest, electric consumption per 1 cell is about 5μA and about 330 mA is consumed for the entire memory array of 60K bit LAM. On the contrary, if a load resistance element of 10^5 MΩ is used in this embodiment, the consumption is only 3.3 mA. This is an example showing the effectiveness for attaining a large capacity memory.

4. Brief Description of the Drawings

Fig. 1 is a cross sectional view for explaining the prior art method, Fig. 2 (a)-(c) are cross sectional views of steps for explaining the method of manufacturing a resistance element in one embodiment according to the present invention, Fig. 3 is a cross sectional view for explaining a wiring system of the resistance element shown in Fig. 2, Fig. 4 is a cross sectional view for explaining another wiring system of the resistance element shown in Fig. 2, Fig. 4 is a cross sectional view for explaining a modified example of the wiring system of the resistance element shown in Fig. 4, Fig. 6 is a cross sectional view for explaining a semiconductor device in which the resistance element shown in Fig. 4 and the MOS type transistor are connected, and Fig. 7 is a circuit diagram when a flip-flop is constituted with the semiconductor

device shown in Fig. 6.

In Fig. 6:

21 ... silicon substrate,

22, 31 ... silicon oxide film,

23 ... polysilicon layer,

25, 25' ... polysilicon electrode,

32' ... AL wiring,

41 ... drain,

61 ... gate oxide film,

62 ... polysilicon gate electrode,

63 ... source.